MODEL 8181
REMOTE DISPLAY
SERIAL NO. 1210, 1221-1

©

SYSTRON DONNER

INSTRUCTION MANUAL

MODEL 8181

REMOTE DISPLAY

SERIAL NO. 1210, 1221-1224

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SYSTRON DONNER CORPORATION

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SYSTRON DONNER
CORPORATION

WARRANTY

This Systron-Donner product is warranted against defects in materials and workmanship for a period of one year from the date of shipment. Systron-Donner will, at its discretion, repair or replace products that prove to be defective during the warranty period provided they are returned to Systron-Donner. Repairs necessitated by misusing this product are not covered by this warranty. This warranty does not apply to certain components, such as vacuum tubes and batteries. These components will only be replaced if warranted by the original manufacturer. No other warranties are expressed or implied, including, but not limited to, fitness for a particular purpose, or merchantability. Systron-Donner is not liable for consequential damages.

INSPECTION AND RETURN

This Systron-Donner product was carefully inspected and in perfect working order at the time of shipment. Each instrument should be checked for proper operation when received. If the instrument is damaged in any way, or fails to operate, a claim should be filed with the carrier immediately.

Should it become necessary to return an instrument to the factory, it should be packaged in its original container (or suitable substitute) and shipped prepaid with documentation stating the reason for return and the service desired.

REPAIRS AND REPLACEMENT PARTS

Whenever an instruement requires service, your nearest Systron-Donner representative should be contacted. All representatives will provide immediate service or, when necessary, arrange for factory return.

Replacement parts for warranty repairs can be obtained without cost by contacting your Systron-Donner representative or from Systron-Donner directly. When ordering parts, please use the identifying Systron-Donner part numbers, and give the model and serial number of the instrument for which they are intended. Return of the defective parts will be requested after repair.

Address all requests or inquiries to your nearest Systron-Donner representative or contact:

SYSTRON-DONNER CORP.
Instrument Division
10 Systron Drive
Concord, Calif. 94518

Phone (415) 676-5000

TWX: 910-481-9479

STANDARD OPTIONS

Standard options installed in your unit are checked below. Circuit descriptions for these options are provided in Chapter 6. Special modifications, when included, are described in Chapter 7.

SERIAL NUMBER

OPTION		DESCRIPTION
C18	☐	NASA 36 Bit Code, in lieu of IRIG A/B.
C47	☐	XR3 (250/1 kHz), in lieu of IRIG A/B.
D11	☐	Parallel BCD Outputs in hours, minutes and seconds.
D11D	☐	Parallel BCD Outputs in days, hours, minutes and seconds.
E13	☐	Days. Adds three digits to the display.
M16	☐	Mounting Yoke, ceiling/wall.
	☐	Transformer Input Option.
	☐	Input Filter Option.
	☑	Special Modification (See Chapter 7).

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TABLE OF CONTENTS

		Page
CHAPTER 1 - GENERAL DESCRIPTION		
1.1	Introduction	1-1
1.2	Specifications	1-1
CHAPTER 2 - INSTALLATION		
2.1	Initial Inspection	2-1
2.2	Storage and Reshipment	2-1
2.3	Power Requirements	2-1
2.4	Yoke Mounting	2-2
2.5	Installation	2-2
CHAPTER 3 - OPERATION		
3.1	General	3-1
3.2	Operating Conditions	3-1
CHAPTER 4 - MAINTENANCE		
4.1	Factory Service	4-1
4.2	Routine Maintenance	4-1
4.3	Printed-Circuit Board Repair	4-2
4.4	Logic Functions	4-2
4.5	Operational Test	4-5
4.5.1	Recommended Test Equipment	4-5
CHAPTER 5 - FUNCTIONAL DESCRIPTION		
5.1	General	5-1
5.2	Power Supply	5-1
5.3	Display Circuitry	5-1
5.4	Input Cycle Detector	5-1
5.5	Time-of-Day Accumulator	5-2
5.6	Reader Logic	5-2
7-071361	Schematic, Time Code Reader Display Model 8181	5-3
7-071453	Schematic, Power Supply	5-4
07136101	Assembly, Interconnect P.C. Board	5-5
07136001	Assembly, Readout P.C. Board	5-6
	Final Assembly Parts List	5-7
021588-7-1	IRIG Reader Logic Circuit Description	5-9
	Schematic	5-10
	Assembly	5-11
	Parts List	5-12
CHAPTER 6 - STANDARD OPTION ADDITIONS		
6.1	General	6-1

Page

CHAPTER 6 - STANDARD OPTION ADDITIONS (Cont'd)

021591-7-1 Option C18 NASA 36 Reader Logic
Circuit Description 6-2
Schematic 6-3
Assembly 6-4
Parts List 6-5

021658-7-1 Option C47 XR-3 Reader Logic
Circuit Description 6-6
Schematic 6-8
Assembly 6-9
Parts List 6-10

7-071449 Option D11/D11D Parallel BCD Outputs
Circuit Description 6-11
Schematic 6-12
Parts List 6-13

7-071361 Option E13 Days
Circuit Description 6-14
Parts List #071475 6-15

7-071454 Transformer Input Option 6-16
Circuit Description 6-16
Schematic 6-17
Parts List #071473 6-18

7-071472 Input Filter Option
Circuit Description 6-19
Schematic 6-20
Parts List #071471 6-21

CHAPTER 7 - SPECIAL MODIFICATIONS

7.1 General 7-1

LIST OF FIGURES

Figure 2.1 3½" Full Rack Assembly #039986-5 2-3

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8181 Remote Display accepts a serial BCD time code on an amplitude-modulated carrier and translates it into parallel form for display in decimal hours, minutes and seconds. Days may be included as an option. The parallel BCD information can also (optionally) be made available as buffered parallel outputs.

The basic Model 8181 translates either the IRIG A (10 kHz carrier) or the IRIG B (1 kHz carrier) time code as selected by an internal switch. Optional codes include NASA 36 Bit (1 kHz carrier) or XR3 (250 Hz/ 1 kHz carrier).

The Model 8181 is used in many applications where translation and display of remote time information is required. It is of particular value where time must be displayed over long distances.

1.2 SPECIFICATIONS

Display: Six-digit, in-line, seven-segment planar readout displays time in hours, minutes and seconds. Numerals are one inch (25 mm) high. Lighted colons are provided between hours and minutes and between minutes and seconds digits. The Days Option adds three digits to the display.

Input Code Format: The basic Model 8181 accepts either the IRIG A or the IRIG B time code. NASA 36 Bit or XR3 (250 Hz/1 kHz) time codes may be accommodated on an optional basis.

Input: The AGC and cycle detector circuits can accept carrier frequencies from 80 Hz to 12 kHz, modulation ratios of 2:1 to 6:1 and voltage levels from 0.25 V to 7.5 V peak-to-peak. The input is single ended with an impedance of greater than 1 M ohm to ground. A floating (transformer coupled) input with a bridging impedance of greater than 10 k ohm at 1 kHz is available as an option. Provision is included for mounting a line terminator and/or input filter.

The single ended input is via a rear panel BNC. A second BNC, connected in parallel, is provided to aid in chain wiring displays. The input is via a rear panel barrier strip when the transformer option is provided.

Outputs: The optional parallel BCD outputs are supplied via a rear panel connector (Amph. 57-40500).

Code: 8-4-2-1

"1" = 5 ±0.5 V behind 6 k Ω

"0" = 0 to +0.5 V, 12 mA sink

Environment:

Operating	0° C (32° F) to 60° C (140° F) at up to 95% relative humidity.
Storage and Shipment	-55° C (-69° F) to 85° C (185° F).

Power: 115/230 volts ±10%, 48 to 440 Hz at less than 15 watts via rear panel three-pin connector. Power cable is supplied.

Dimensions: 3½"H x 19"W x 9-1/8"D (8.9 x 48.3 x 23.2 cm). Removable rack handles.

Weight: 9 lbs. (4.1 kg) net, 11 lbs. (k kg) shipping.

Package: The Model 8181 Remote Display is normally supplied as a 3½ by 19-inch rack mount panel which compliments all new Systron-Donner 8000 Series timing units. Removable rack handles allow the display to be operated on the bench or with the optional all-angle swivel yoke assembly. In this configuration the width is reduced to 16-3/4 inch (42.5 cm).

CHAPTER 2
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found, refer to the warranty at the front of this manual and to Section 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 180°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General Packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb.sq.in. bursing strength) or wooden box to house the instrument.

3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER REQUIREMENTS

The Model 8181 can operate from 115 V or 230 V ±10%, 48 to 440 Hz, 15 watts. The unit is normally supplied for 115 volt operation.

To adapt the Model 8181 to 230 volt operation, remove the jumper wire between pins 1 and 2 and also pins 3 and 4 of the main power transformer (T1). Install a jumper wire between pins 2 and 3 of the main power transformer.

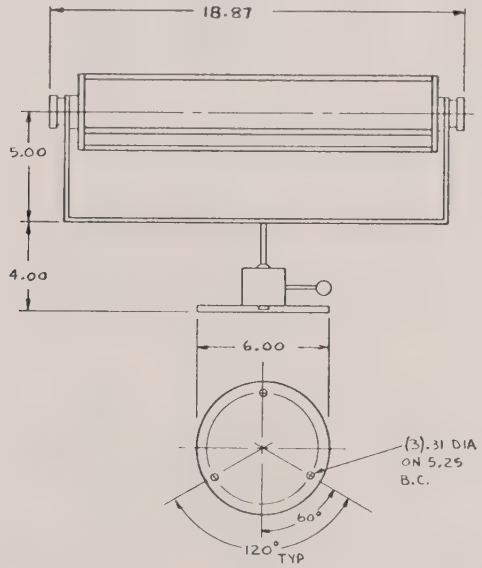
CAUTION

Disconnect all power from the unit before changing voltages.

2.4 YOKE MOUNTING

The instrument is normally supplied for bench top or rack mounted operation. If yoke mounting is desired (Option M16), the following steps are necessary:

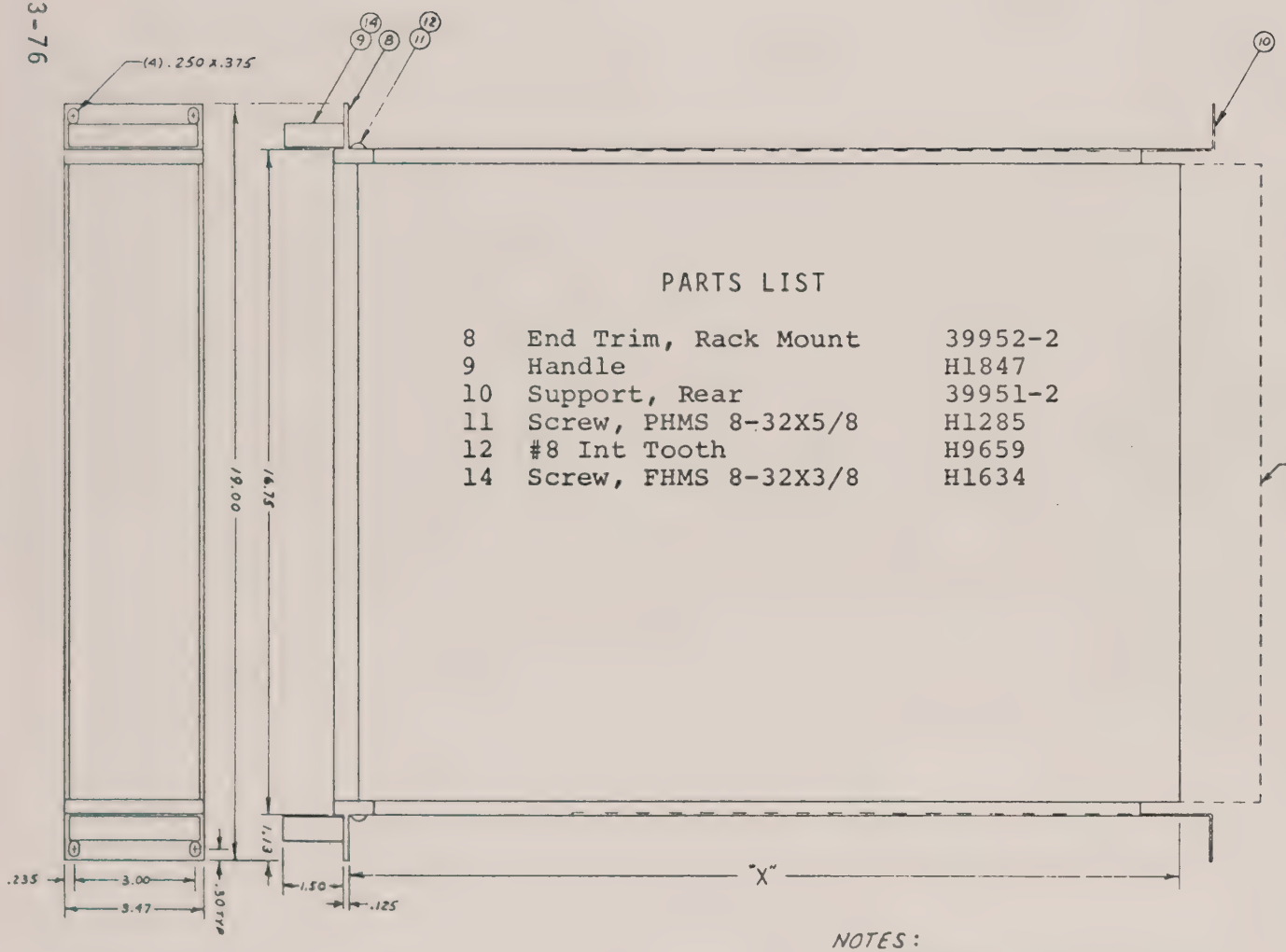
1) If supplied for rack mount, remove the rack mounting ears.
2) Drill three holes in mounting surface to accommodate yoke base, and bolt the base into position.
3) Insert the unit into the yoke fork and attach the unit to the fork with two wing bolts (supplied).
4) Insure that enough slack is present in the signal cable and power cord to allow the unit to rotate a full 360 degrees.



YOKE MOUNTING OPTION #021814

2.5 INSTALLATION

Mount as desired, connect to the proper power source (refer to 2.3), and make the interconnection between the Model 8181 and the signal source.



PARTS LIST

8	End Trim, Rack Mount	39952-2
9	Handle	H1847
10	Support, Rear	39951-2
11	Screw, PHMS 8-32X5/8	H1285
12	#8 Int Tooth	H9659
14	Screw, FHMS 8-32X3/8	H1634

TABULATION

P/L #	"X"	INSTR. DEPTH
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

NOTES:
1. INSTR. ARE DRILLED TO ACCEPT 20" JONATHAN 120 QD SERIES SLIDES
2. ITEM 10 DELETED WHEN SHIPPED W/SLIDES

FIGURE 2.1 3½" FULL RACK ASSEMBLY #039986-5 REV A

CHAPTER 3
OPERATION

3.1 GENERAL

Since the Model 8181 is a fully automatic instrument, no preliminary adjustments are required and no operator controls are provided. An internal switch permits selection of the IRIG A or IRIG B Time Code on the basic unit, or XR3 250 Hz or 1 kHz when Option C47 is included.

The only steps necessary to bring the unit to a fully operational condition are to install the signal cable and power cord.

3.2 OPERATING CONDITIONS

Maximum Temperature: 140°F (60°C)

Minimum Temperature: 32°F (0°C)

CHAPTER 4
MAINTENANCE

4.1 FACTORY SERVICE

Whenever the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquiries on operation or applications to your nearest sales representative, or Sales Manager:

SYSTRON-DONNER CORPORATION
DATA PRODUCTS DIVISION
935 Detroit Avenue
Concord, California 94518
Phone: (415) 798-9900
TWX: 910-481-5780
Cable: SYSTRONDONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.

2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose or burned wires.

3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed-circuit board contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operation Test Procedure (Section 4.5). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component.)

3) Apply heat (40-50 W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4) Form the tinned leads of the replacement part and insert in the printed circuit holes; solder, then trim leads to extend 1/16-inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16-inch diameter.)

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

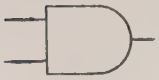
5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the soldered connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.4 LOGIC FUNCTIONS

The logic symbols and functions, as used in the Model 8181, are described in the following paragraph. Truth tables and detailed explanations are given where necessary in order to assist qualified maintenance personnel in the repair and upkeep of the instrument.

AND Gate



OR Gate

NAND Gate

INVERTED OR Gate

The NAND Gate and the INVERTED OR Gate have the same truth tables.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

INVERTED AND Gate

NOR Gate

The NOR Gate and the INVERTED AND Gate have the same truth tables.

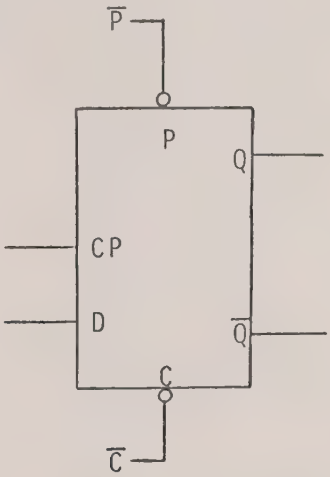
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

DOT AND

DOT OR

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together. These functions are called DOT AND and DOT OR functions.

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) $\overline{P}$ and $\overline{C}$ override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At preset condition, Q is a Logic 1. At a clear condition Q is a Logic 0.

4.5 OPERATIONAL TEST

In the event of an equipment malfunction, the schematics and circuit descriptions in Chapter 5 will aid the technician in isolating the trouble to a particular circuit.

WARNING

Dangerous high voltages are present in the power supply and display circuits of this equipment. Use caution at all times when the protective covers are removed.

4.5.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8181.

Model	Manufacturer	Description
546	Tektronix	Oscilloscope 50 MHz bandwidth triggered sweeps from 0.1 µs/cm to 5 sec/cm.
1A2	Tektronix	Dual-Trace Calibrated preamp for 546 scope, 0.05 volts/cm to 20 volts/cm.
6012	Tektronix	Probe, 10:1 Attenuation Ratio, 12 pF capacitance.
7004A	Systron-Donner	DMM, 10 MΩ input impedance, ±0.1% accuracy.
8150	Systron-Donner	Time Code Generator.

CHAPTER 5
FUNCTIONAL DESCRIPTION

5.1 GENERAL

The Model 8181 Remote Display is shown on Schematic 7-071361. Power supply circuits are shown at the upper left on the schematic. Input cycle detector circuits are shown at the lower left. The reader logic (in block form), time-of-day accumulator and related display circuits are shown at left center. The optional days accumulator and related display circuits are shown on the right. All these circuits are contained on a single P.C. Board with the exception of the display tubes (shown in dotted outline at the top of the schematic) and the plug-in Reader Card, A1. The display tubes are mounted in sockets on a separate P.C. Board which is connected to the main board through right angle pin assemblies. A portion of the power supply (Schematic 7-071453) is mounted on the rear panel.

5.2 POWER SUPPLY

The power supply consists of the ac input connector, line filter, fuse and transformer shown on Schematic 7-071453 plus the circuitry shown at upper left on Schematic 7-071361. Diodes CR17 and CR18 supply unregulated +10 volts to voltage regulator Q3 and (via filter C15, L2, C12) to amplifiers U31 and U32. Voltage regulator Q3 supplies regulated +5V via filter C14, L3, C10 as the Vcc supply to all I.C.'s in the unit. Diodes CR15 and CR16 supply unregulated -10 volts to amplifiers U31 and U32 via filter L1, C11.

Bridge CR9-CR12 provides unregulated +210 volts through fuse F2 (located on P.C. Board) to the AGC circuit and to series pass transistor Q2. The regulated +180 V output from Q2 is fed to the display tubes.

5.3 DISPLAY CIRCUITRY

In the basic unit, parallel BCD time-of-day (T.O.D.) data from accumulator U2-U7 are fed to display drivers U13-U18. The display drivers decode the 8-4-2-1 BCD and drive 7-segment display tubes V1-V6. Since T.O.D. in hours, minutes and seconds is displayed, colons within V3 and V5 are lit by grounding the COL inputs to these tubes through R10-R13. (The 40S, 40M, 40H and 80H inputs to the display drivers are connected to ground.)

The Days Option (E13) adds display drivers U8-U10, display tubes V7-V9 and related components. The colon in V7 is lit via R14 and R15.

5.4 INPUT CYCLE DETECTOR

The circuitry is shown at the lower left on the schematic. The modulated input signal from J2/J3 is fed to source follower Q1. Q1 is required to drive the low impedance detector circuits. Diodes CR3 and CR4, capacitor C5 and resistors R9 and R10 make up the lower large cycle detector which functions as follows: C5 charges to the negative peaks of the large cycles in the code. Approximately 90% of the voltage across C5 appears at the junction of R9 and R10. This sets

the bias on CR3 so that the remaining 10% of the peak signal will pass to the input of U32. Since the small cycles are much less than this, only the lower large cycle peaks are conducted through CR3 to the amplifier. The amplifier is built with positive and negative limiters in the feedback to limit the output swing and prevent overload when input signal levels are high. The clipped (rectangular) waveform at the output is fed through schmitt trigger U1-8 to the Reader Logic card. This $\overline{\text{LLC}}$ signal from U1-8 goes low whenever a lower large cycle peak is detected.

Amplifier U31 is fed the modulated code from Q1. It has sufficient gain for the limiters to take effect even when low level small cycles are present thus producing an output which is a square wave at the carrier frequency. This signal is fed to the Reader Logic card through schmitt trigger U1-11 as the each cycle (EC) input.

5.5 TIME-OF-DAY ACCUMULATOR

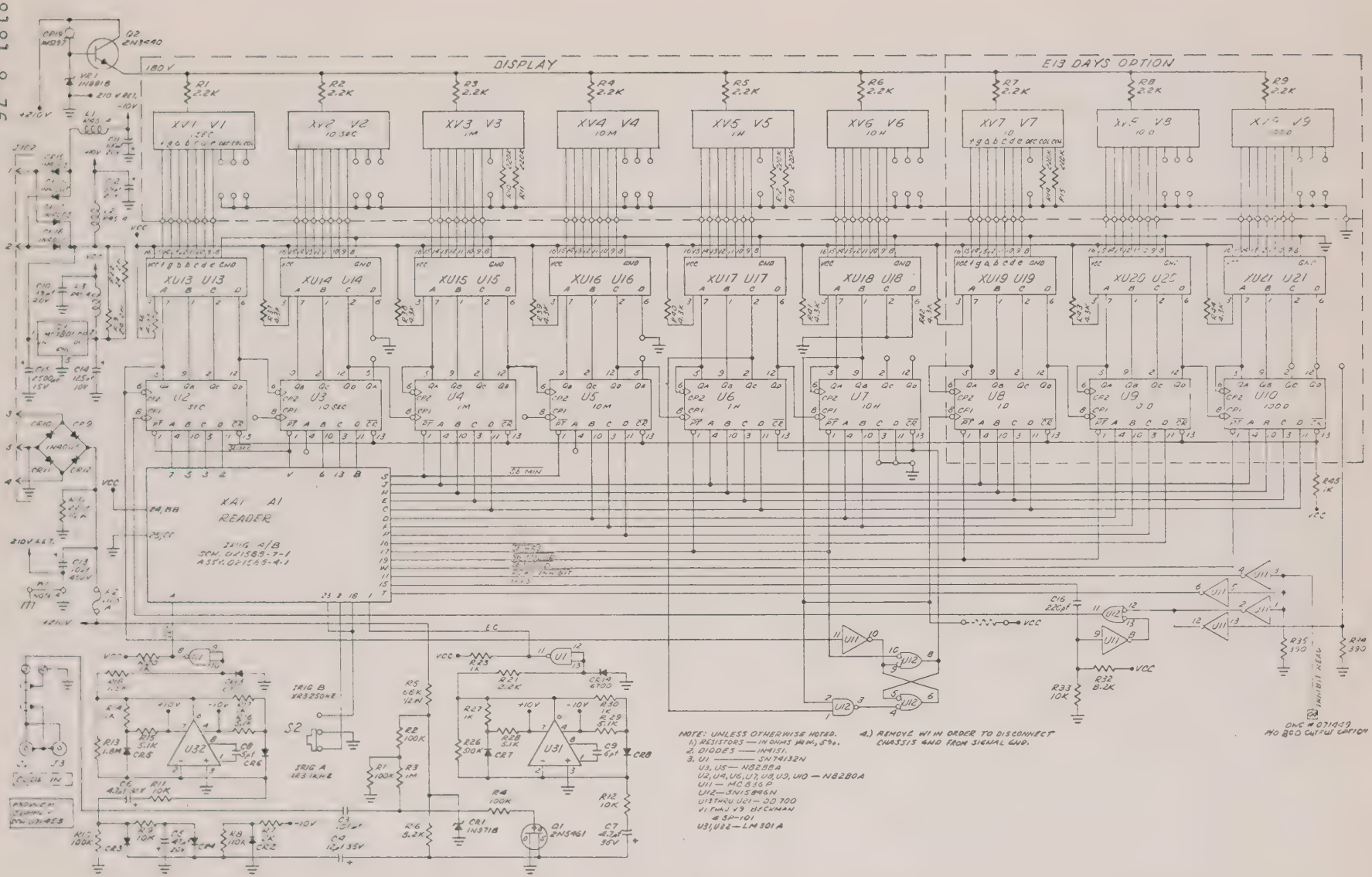
This circuit consists of counters U2-U7. Counters U2,U4,U6 and U7 are divide-by-10. Counters U3 and U5 are divide-by-6. They are connected in tandum to form a circuit which accumulates time in seconds, minutes and hours by counting a 1 pps input derived from the input time code by the Reader Logic. The Reader Logic synchronizes the time in the accumulator to the input code by loading the time stripped from the code into the counter parallel data inputs in seconds, minutes and hours bytes. Once synchronization is achieved the 1 pps update advances the accumulator "on time". The accumulator outputs parallel 8-4-2-1 BCD to the display drivers and (optionally) through buffers as parallel BCD from the unit (see Chapter 6).

The 1 pps input is fed to the accumulator through an inhibit circuit formed from gate U12-11 and inverters on U11. The BCD output option must be included to gain access to this circuit.

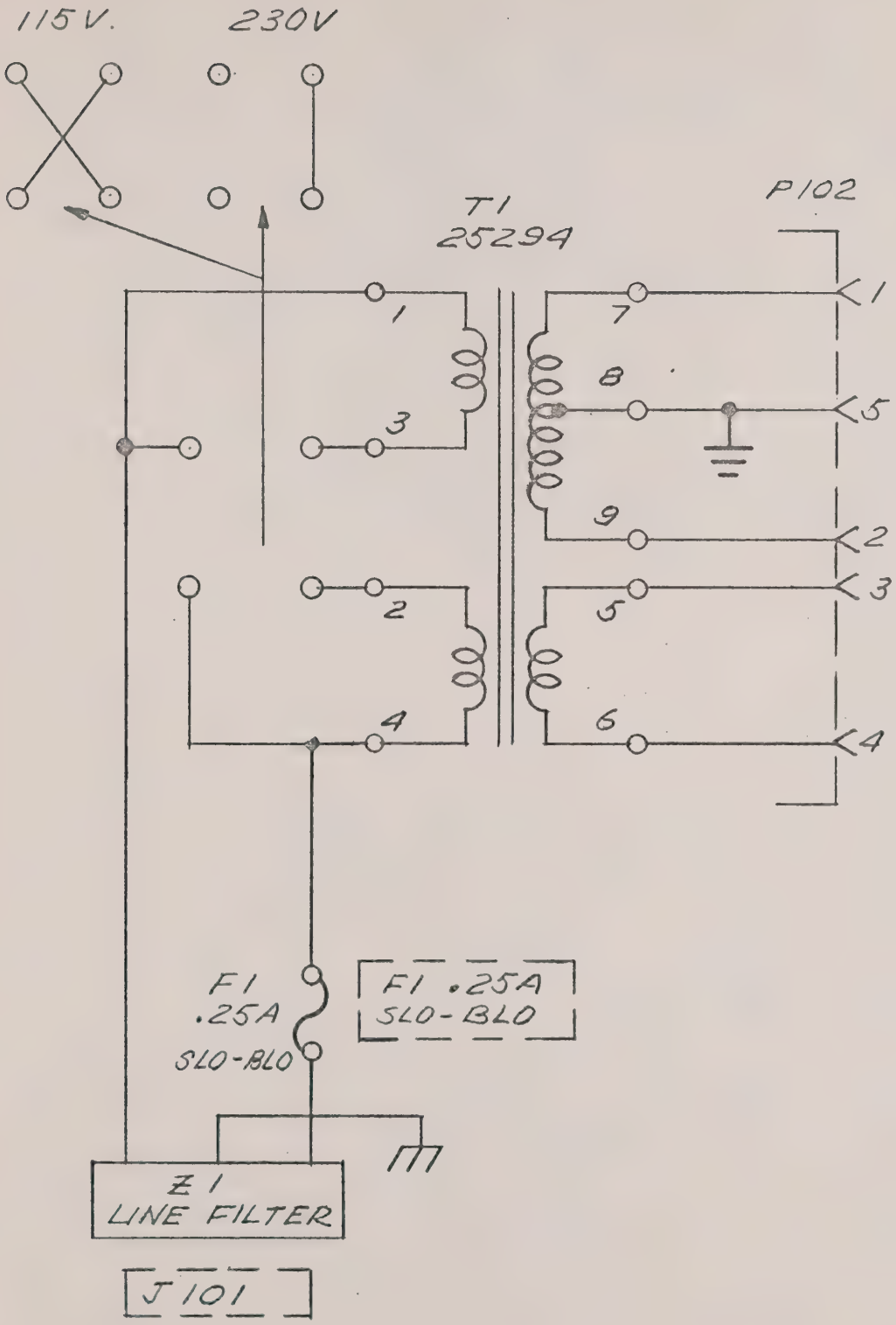
An hours recycle circuit, formed from gates on U12 and inverter U11-10, automatically resets the hours counter to zero at a count of 24. The output from U12-3 goes low at a count of 24 hours setting flip-flop U12-8,6. The U12-8 output resets the hours counter. The flip-flop is cleared through U11-10 when the next 1 pps update occurs.

5.6 READER LOGIC

The basic Model 8181 translates the IRIG B Time Code. This is done by the 021588-4-1 IRIG Reader Logic Card A1. A complete description of this card is provided at the end of this chapter. Optional code Reader Logic cards are described in Chapter 6. To change codes it is only necessary to change Reader Logic cards.

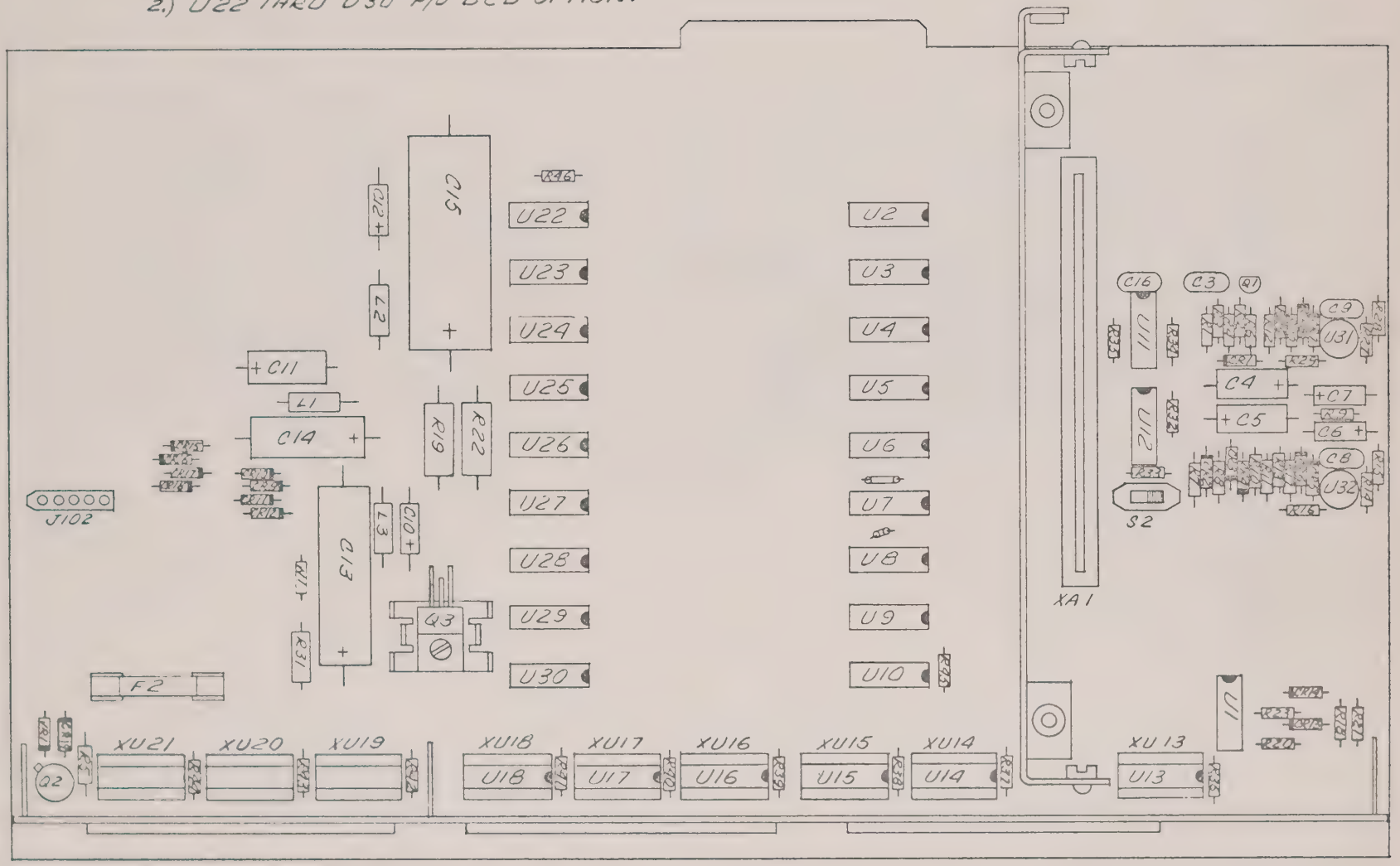

DISPLAY
E13 DAYS OPTION
READER
NOTE: UNLESS OTHERWISE NOTED.
1.) RESISTORS — IN OHMS 1/4W, 5%.
2. DIODES — IN4151.
3. U1 — SN74132N
U3, U5 — N8288A
U2, U4, U6, U7, U8, U9, U10 — N8280A
U11 — MC836P
U12 — SN15896N
U13 THRU U21 — DD 700
V1 THRU V9 BECKMAN 4 SP-101
U31, U32 — LM 301A
4.) REMOVE W1 IN ORDER TO DISCONNECT CHASSIS GND FROM SIGNAL GND.
IRIG B
IRIG A
INHIBIT READ
DWG # 071459
NO BCD OUTPUT OPTION

SCHEMATIC TIME CODE READER DISPLAY MODEL 8181 #7-071361 REV B



SCHEMATIC POWER SUPPLY #7-071453 REV B

NOTE:
1.) U8, U9 & U10 P/O DAYS OPTION.
2.) U22 THRU U30 P/O BCD OPTION.



ASSEMBLY INTERCONNECT P.C. BOARD #07136101 REV C

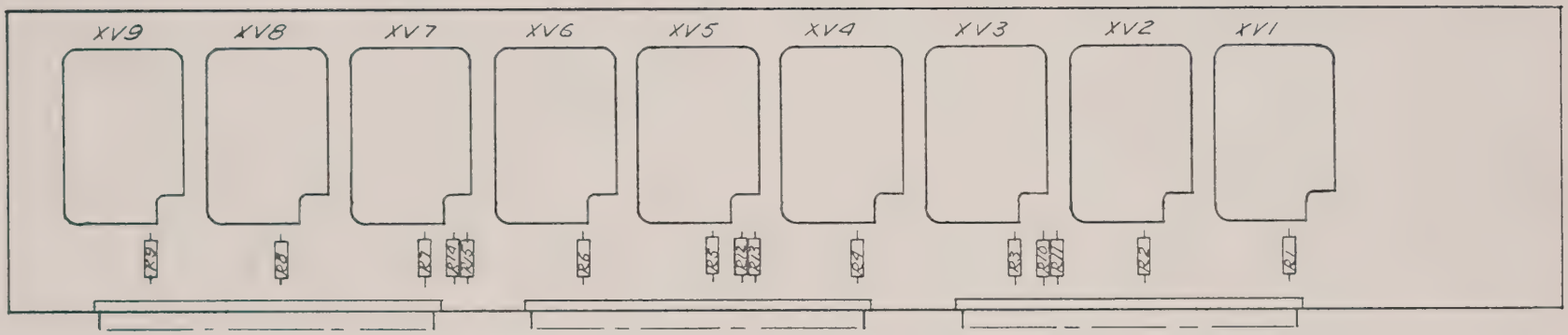
PARTS LIST

INTERCONNECT BOARD #07136101 REV. B_2

REF.	DESCRIPTION	SD PART NO.
	Assembly, Interconnect Board	07136101
	Schematic	7-071361
	Assembly, Readout	07136001
C3	Capacitor, .01µF 100V Disc.	100103
C4	Capacitor, 12µF 35V, Tant	100320
C5	Capacitor, 47µF,20V, Tant	100186
C6,C7	Capacitor, 4.7µF,35V,Tant	100071
C8,C9	Capacitor, 5pF,500V,Mica	100218
C10,C12	Capacitor, 39µF,20V,Tant	102561
C11	Capacitor, 100µF,20V,Tant	100208
C13	Capacitor,10µF,450V,Tant	100062
C14	Capacitor,125µF,10V,Tant	100246
C15	Capacitor,2500µF,15V,Tant	100247
C16	Capacitor,220pF,500V,Mica	100220
CR1	Diode, 1N971B	100402
CR2,3,4, 5,6,7,8	Diode,1N4151	100385
CR9,10,11, 12,15,16, 17,18	Diode,1N4005	100413
CR 13,14	Diode,6700	006700
CR 19	Diode,1N5297	100457
F2	Fuse, .125A	100592
L1,2,3	Inductor, R45-4	101313
Q1	Transistor,2N5461	101383
Q2	Transistor,2N3440	101420
Q3	Transistor,MC7805CP	045256
	Heat sink IERC PA1-1CB	100978
R1,2,4,10	Resistor,100K,¼W.,5%,CC	101558
R3	Resistor,1M,¼W,5%,CC	101605
R5	Resistor,68K,½W,5%,CC	101462
R6,32	Resistor,8.2K,¼W,5%,CC	101595
R7	Resistor,2K,¼W,5%,CC	101553
R8	Resistor,110K,¼W,5%,CC	101617
R9,11,12, 33	Resistor,10K,¼W,5%,CC	101570

PARTS LIST
INTERCONNECT BOARD (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R13	Resistor,1.8M,¼W,5%,CC	101759
R14,17,20,23, 27,30,45	Resistor,1K,¼W,5%,CC	101569
R15,16,28,29	Resistor,5.1K,¼W,5%,CC	101541
R18	Resistor,1.5K,¼W,5%,CC	101577
R19,22	Resistor,24Ω,2W,5%,CC	106040
R21	Resistor,2.2K,¼W,5%,CC	101562
R26	Resistor,510K,¼W,5%,CC	101611
R31	Resistor,220K,½W,5%,CC	101458
R34,35	Resistor,390Ω,¼W,5%,CC	101592
R36-44	Resistor,4.3K,¼W,5%,CC	101546
S2	Switch,S.P.D.T.	102325
U1	Integrated Circuit,SN7413 2N	045270
U2,4,6,7	Integrated Circuit,N8280A	025722
U3,5	Integrated Circuit,N8288A	025723
U11	Integrated Circuit,MC836P	025704
U12	Integrated Circuit,SN15846N	019716
U13,14,15,16, 17,18	Integrated Circuit,DD700	045203
U31,32	Integrated Circuit,LM301AH	025745
W1	Jumper,Molded	102879
VR1	Diode,1N991B	100461
XA1	Connector,50 Pin,252-25-30-012	101239
XJ102	Recpt.Shell,Molex 03-06-1055	101264
XU13-21	Socket,16 Pin	103350
	Bracket Display Board	051450
	Card Guide	021340-1-2
	Card Guide Bracket	071356
	Contact Male,Molex 02-06-8103	10282203
	Fuse Clip	102745



ASSEMBLY READOUT P.C. BOARD #07136001 REV B_1

PARTS LIST

READOUT BOARD #07136001 REV B_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	07136001
R1-9	Resistor, 2.2 k 5%, ¼ W, CC	101562
R10-15	Resistor, 220 k 5%, ¼ W, CC	101610
	Connector, 30 pin	101277
XV1-XV9	Socket,Beckman C5-101	116083

PARTS LIST

FINAL ASSEMBLY #071367

REF.	DESCRIPTION		SD PART NO.
	Final Assembly		071367
	Test Assembly		071366
	Side Trim		03985901
	End Trim, Rack Mount		03995202
	Top Cover		03376001
	Handle		100927
	Nomen Panel		071349
	Window		071350
	Trim Strip		071464
	Trim Strip Insert		071428
	Front Trim		033762
	Bracket		039857
	Nut Tinnerman		100959
	Cord, Vinyl		100955
	Line Cord		102407
	Assembly, Wall Mount (M16)		071469
	Assembly, Bench Mount		071488
	Assembly, BCD Output (D11/D11D)		
	Assembly, Days (E13)		071475
	Assembly, NASA 36 (C18)	(021591-7-1)	071495
	Assembly, XR3 (C47)	(021658-7-1)	071496
	Assembly, Input Transformer		071473
	Assembly, Filter		071471
	Test Assembly		071366
A1	Assembly, Reader Card, IRIG B		021588-4-1
	Assembly, Interconnect		07136101
	Assembly, Rear Panel		071364
	Schematic		7-071361
	Front Panel, Sub		071348
	Gusset		071357
	Bracket, P.C. Board, Left		07135202
	Bracket, P.C. Board, Right		07135201
V1-6	Beckman Display, SP-101		116082
	#6-32 x 7/16" F.H.M.S		10073107
	#6-32 x 5/16" P.H.M.S		10063205
	#6 Flat Washer		100662
	#6 Split Lockwasher		100712
	#8-32 x 1/4" F.H.M.S		10074304

PARTS LIST

FINAL ASSEMBLY (Cont'd)

REF.	DESCRIPTION	SD PART NO.
	Assembly, Rear Panel	071364
	Schematic, Time Code Reader	7-071361
	Schematic, Power Supply	7-071453
F1	Fuse, ¼ A Slo-Blo	100600
XF1	Fuse Holder	102409
J2,3	Connector, BNC	101155
J101	Receptacle w/filter	102461
	Connector, Cover Plate	071355
P102	Plug Shell, Molex 03-06-2055	101263
	Contact, Female, Molex 02-06-1132	
T1	Transformer	025294
	Insulator, BNC	100823
	Ground Lug	100495
	Transformer Mounting Bracket	116085
	#4-40 x ¼" P.H.M.S.	10062604
	#4-40 Kep Nut	100941
	#4 Ground Lug	102827
	#6-32 x ¼" P.H.M.S	100712
	#6 Split Lockwasher	100712
	#8-32 x 3/8" P.H.M.S.	10064206
	#8 Kep Nut	100940

CIRCUIT DESCRIPTION
IRIG READER LOGIC
SCHEMATIC #021588-7-1

1) GENERAL

The IRIG Reader Logic card accepts the Lower Large Cycle ($\overline{LLC}$) and Each Cycle (EC) signals from the AGC and Cycle Detector and detects the ONES, ZEROS and MARKS in the code. It sorts out the BCD time information and loads it into a shift register in two-digit bytes. These data are transferred, in parallel, to the Time Accumulator by Strobe signals generated on the card.

2) FUNCTION

When a MARK is detected, the nine-bit shift register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" counter A10 is advanced one.

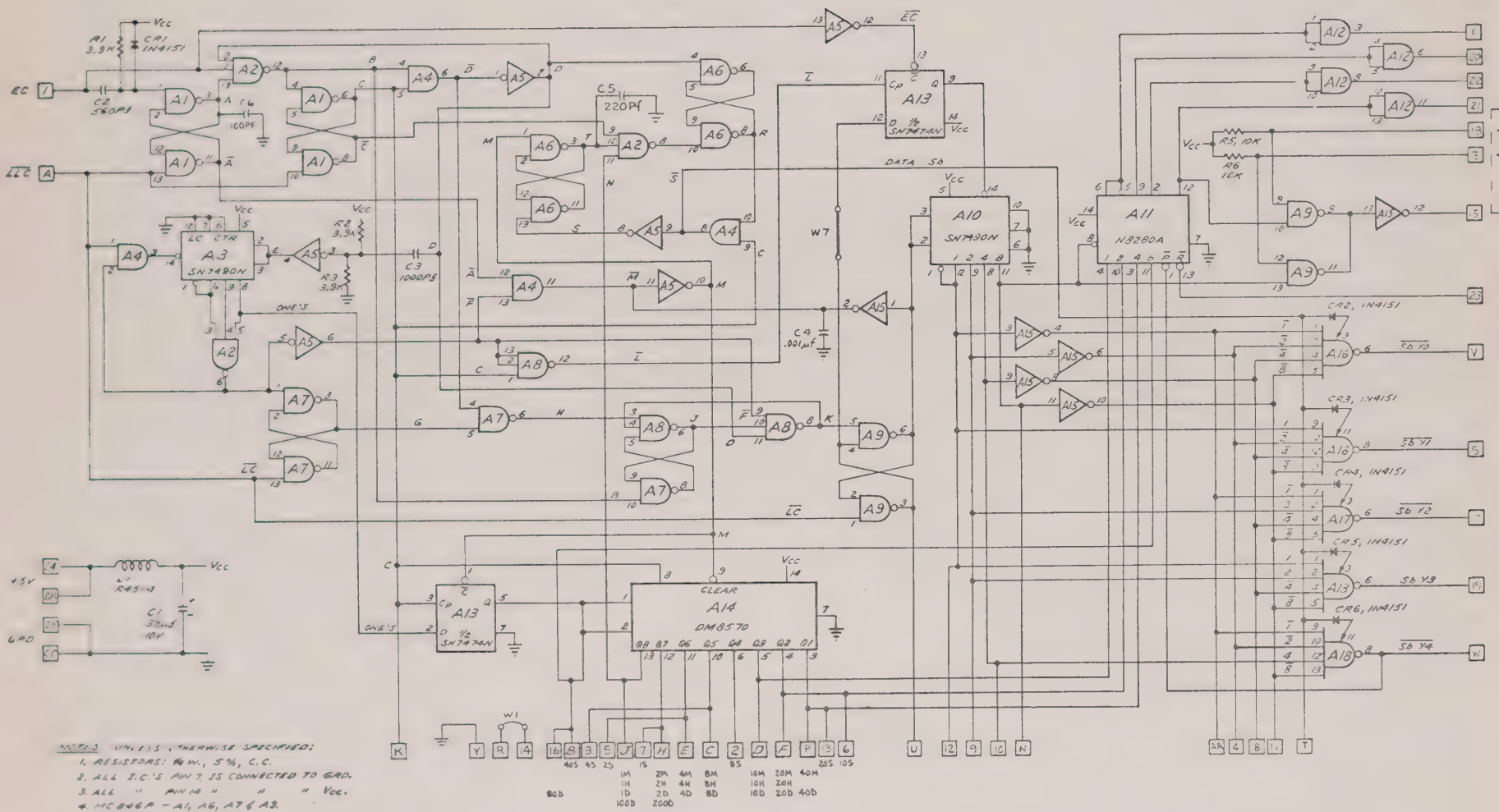
When the second MARK of the double MARK is detected, the sequence is changed so that the "Y" counter is set to ZERO if it was not already at ZERO. It is not advanced for this MARK. Nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the Time Accumulator.

When the next MARK is detected, the register is cleared, a ONE entered and the "Y" counter advanced one. After nine bits are shifted into the register the information is transferred to the minutes section of the Accumulator. This cycle of operation is repeated a third time for hours information. If Days are included, two additional cycles transfer this information to the Accumulator. The "Y" counter continues to count MARKS throughout the time frame.

When the first MARK of the next double MARK is detected, it steps the "Y" counter from 9 to zero advancing the Time Accumulator one second. It is thu updated at the beginning of the frame and will contain the same information (assuming no errors) scanned in during the frame. (The readout does not change during scan-in since the Accumulator is already updated.)

Provision is made through decade A11 and gates on A9, to select 1 pps at pin 15 for the IRIG A and IRIG B codes. Decade A11 is synchronized with the tenths-of-seconds in the IRIG A code by the $\overline{SbY4}$ output from A18-8. Tenths-of-seconds are then available at the outputs from A12.

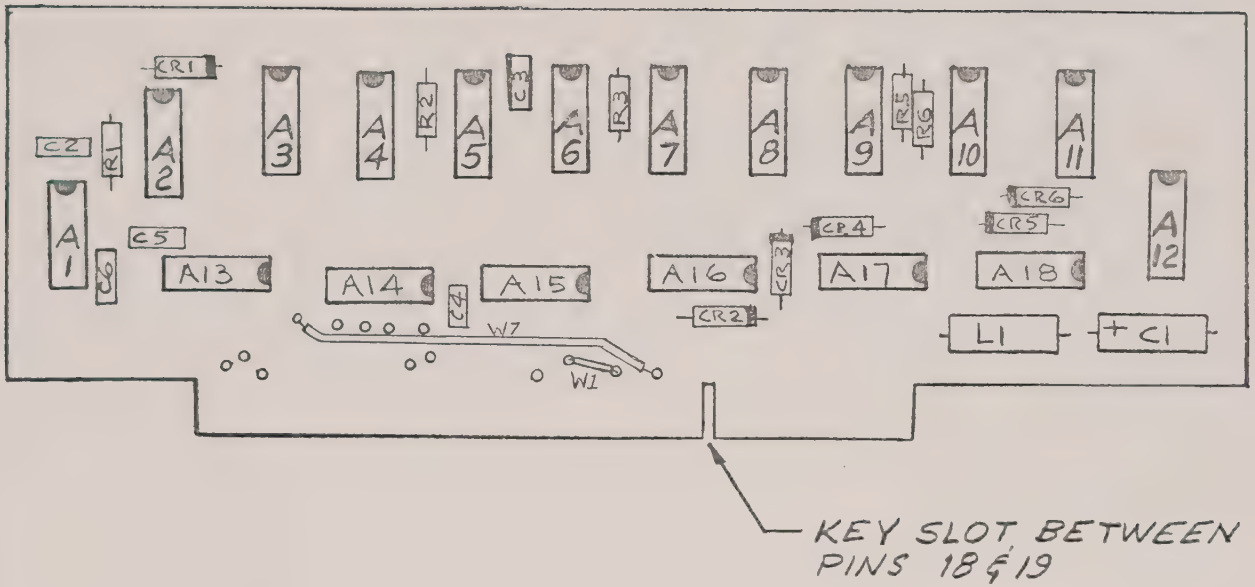
Jumpers are provided to output the ONES signal from A3-8 (pin R), the $\overline{Clear}$ signal ($\overline{M}$) from A4-11 (pin 14) and the Y-Counter input signal from A13-9 (pin M).



NOTES UNLESS OTHERWISE SPECIFIED:

1. RESISTORS: ¼ W., 5%, C.C.
2. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
3. ALL " PIN 14 " " " Vcc.
4. MC 846P - A1, A6, A7 & A9.
   MC 863P - A2 & A8.
   MC 1806P - A4 & A18.
   MC 839P - A5 & A15.
   MC 830P - A16, A17 & A18.

IRIG READER LOGIC SCHEMATIC #21588-7-1 REV C



IRIG READER LOGIC ASSEMBLY #021588-4-1 REV D

PARTS LIST

READER LOGIC #021588-7-1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021588-4-1
	Schematic	021588-7-1
A1,6,7,9	Integrated Circuit, MC846P	019716
A2,8	Integrated Circuit, MC862P	019719
A3,10	Integrated Circuit, SN7490N	025732
A4,12	Integrated Circuit, MC1806P	025733
A5,15	Integrated Circuit, MC836P	025704
A11	Integrated Circuit, N8280A	025722
A13	Integrated Circuit, SN7474N	025241
A14	Integrated Circuit, DM8570	025751
A16-18	Integrated Circuit, MC830P	019712
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, 300 V	100222
C3	Capacitor, .001 µF, 100 V	100243
C4	Capacitor, .001, 1 kV	100076
C5	Capacitor, 220 pF, 500 V	100220
C6	Capacitor, 100 pF, 600 V	100173
CR1-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W	101601
R5,6	Resistor, 10 k 5%, 1/4 W	101570
W1-7	Jumper, Insulated #24 guage	
	Extractor	100865

CHAPTER 6
STANDARD OPTION ADDITIONS

6.1 GENERAL

The standard options available for inclusion in the Model 8181 are described in this chapter. These include the following:

Option C18: NASA 36-Bit Time Code. Substitues a #021591-4-1 NASA Reader Card for the #021588-4-1 IRIG Reader Card normally supplied.

Option C47: Switch selectable XR3 250 Hz or 1 kHz Time Code. Substitutes a #021658-4-1 XR3 Reader Card for the #021588-4-1 IRIG Reader Card normally supplied.

Option D11: Parallel BCD Outputs in hours, minutes and seconds. Adds a rear panel connector and six buffer chips to the basic unit.

Option D11D: Parallel BCD Outputs in days, hours, minutes and seconds. Adds a rear panel connector and nine buffer chips to the basic unit. Days Option E13 is a prerequisite.

Option E13: Days. Adds three accumulator decades, three display drivers and three display tubes to the basic unit.

Transformer Input Option.

Input Filter Option.

CIRCUIT DESCRIPTION
NASA 36 READER LOGIC (OPTION C18)
SCHEMATIC #021591-7-1

1) GENERAL

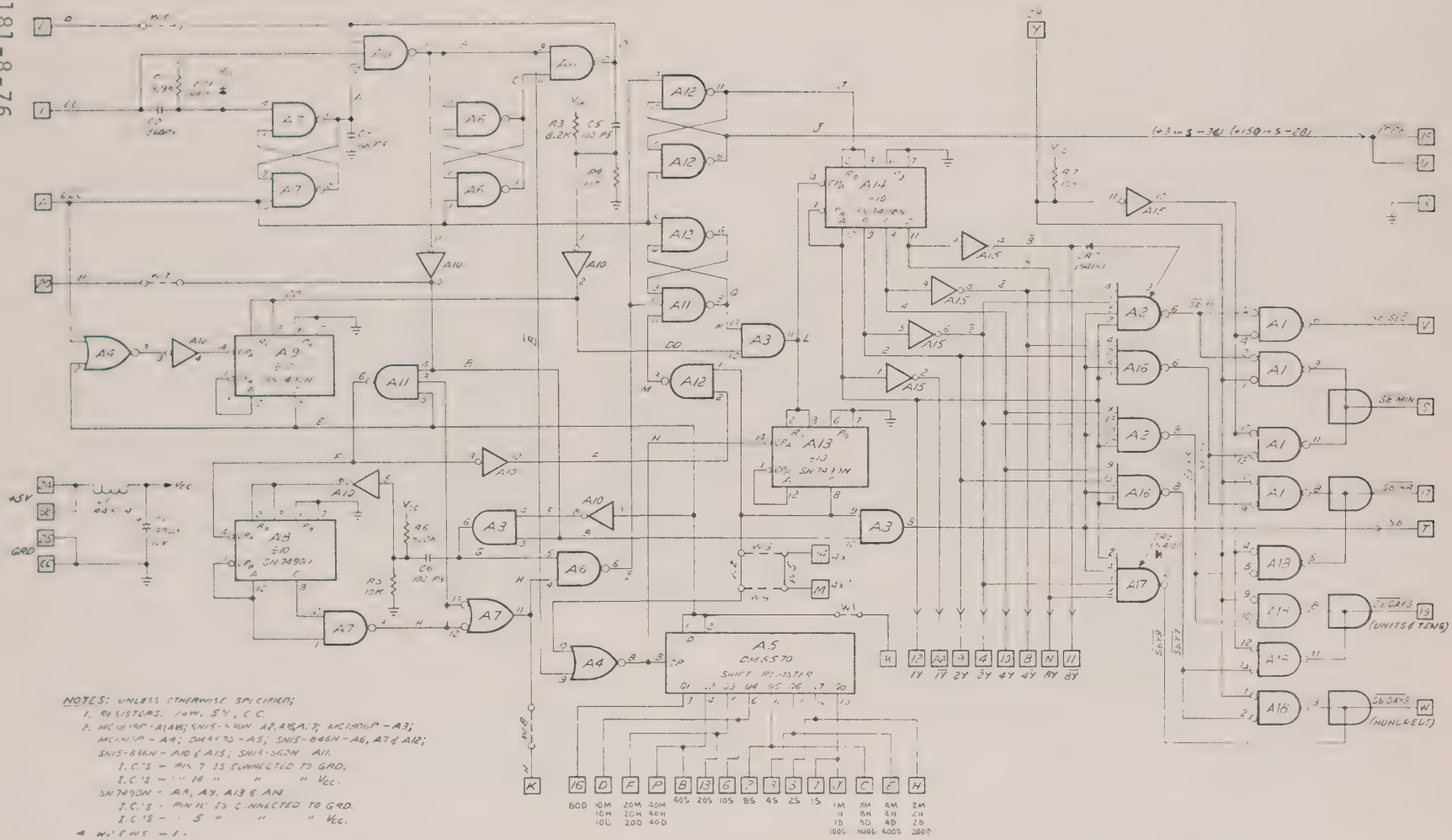
The NASA Reader Logic Card accepts the EC and $\overline{LLC}$ signals from the AGC and Cycle Detector, and detects the ONES, ZEROS and MARKS in the code. Signals are developed to shift the BCD time information on the input code into a shift register and then transfer it to the Time-of-Day Accumulator which drives the display.

2) FUNCTION

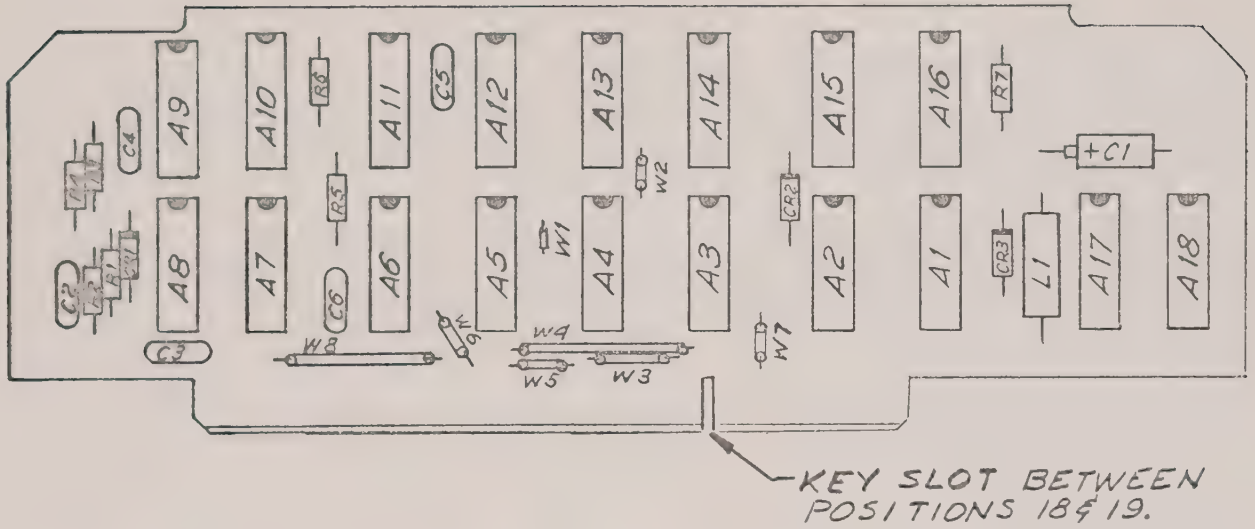
Flip-flops A7-6,8; A6-11,3; and interlocked flip-flop A11-12 and A6-8 serve to extract the (delayed) modulation envelope from the time code. The envelope signal from A11-12 is used to clock shift-register A5 and to advance "X" counter A13 one count for each bit. The leading edge of this signal is differentiated in C5, R3, R4 and used to reset the bit-length counter A9 so that starting from reset (i.e. at the beginning of a bit), it counts the number of Lower Large half cycles in the bit. When this count is less than 4, the bit is called a "zero"; more than 4, a "one". The "one" output, A9-8, is applied to the data input of shift register A5 and to ones counter A8 which serves at the frame mark detector. A8 and associated gating detects five or more consecutive "ones" and, upon the next "zero" set frame resets flip-flop A12-8,11.

In addition to the shift-register outputs, signals are also supplied to gate the shift-register data into external seconds, minutes and hours registers. These strobe signals are obtained by gating the C (or 4) output of "X" counter A13 with the inverse of the envelope signal. The resulting signal is then gated with the A, B, C and D (or 1, 2, 4 and 8) outputs of "Y" counter A14 to produce for the 36-bit code, the seconds strobe pulse at A2-6, the minutes strobe at A16,-6, and the hours strobe at A2-8. These strobe pulses are gated to pins V, S and 17 through gates on A1. (Note: Days strobe signals are developed in gates A16-8 and A17-6, then are gated to pins 19 and W through gates on A18. In addition, provision is made through pin Y and inverter A15-10 to shift all strobe signals one Y-time lower, when reading a NASA 28-bit code. These circuits are not used in the Model 8030.

"X" counter A13 counts once for each bit and is constrained to a maximum count of five (equivalent to BCD digit) by gate A4-8. In this way A13 remains locked-up (and also shift register A5) until reset by the action of flip-flop A12-6, A11-8 in detecting the 10 pps index markers in the time code just before the next BCD digit. The "Y" counter A14, counts once for each BCD digit (i.e. once for each cycle of the "X" counter) when operating with a forward input code.



SCHEMATIC NASA 36 READER LOGIC #021591-7-1 REV F_1



W2 & W5 – 1
W1, W3, W4, W6, W7, W8 –

ASSEMBLY NASA 36 READER LOGIC #021591-4-1 REV C

PARTS LIST

NASA 36 READER LOGIC #021591-4-1 REV D

REF.	DESCRIPTION	SD PART NO.
	Assembly	021591-4-1
	Schematic	021591-7-1
A1,18	Integrated Circuit, MC1808P	025734
A2,16,17	Integrated Circuit, SN15830N	019712
A3	Integrated Circuit, MC1806P	025733
A4	Integrated Circuit, MC1810P	025735
A5	Integrated Circuit, DM8570	025751
A6,7,12	Integrated Circuit, SN15846N	019716
A8,9,13,14	Integrated Circuit, SN7490N	025732
A10,15	Integrated Circuit, MC836P	025704
A11	Integrated Circuit, SN15862N	019719
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF	100222
C3,5,6	Capacitor, 100 pF, 500 V	100173
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1	Resistor, 3.9 k 5%, ¼ W	101601
R3,6	Resistor, 8.2 k 5%, ¼ W	101595
R4,5,7	Resistor, 10 k 5%, ¼ W	101570
W2,5	Wire, 24 gauge Wire, Teflon sleeving	

CIRCUIT DESCRIPTION
XR-3 READER LOGIC (OPTION C47)
SCHEMATIC #021658-7-1

1) GENERAL

The XR-3 Reader Logic accepts the EC and $\overline{LLC}$ signals; sorts out MARKS, ONES and ZEROS; accumulates the serial time data in a serial-in/parallel-out shift-register; transfers the contents of the shift-register into an Accumulator in bytes; and updates this Accumulator at the beginning of each frame maintaining it "on time". A large cycle (LC) counter divides the $\overline{LLC}$ signal by four when operating with an input on a 1 kHz carrier.

In the XR-3 Time Code Format, a REFERENCE MARK is 36 ms long and consists of nine large cycles when constructed on a 250 Hz carrier. A ONE is 24 ms or six large cycles and a ZERO is 12 ms or three large cycles. The 20 bits, representing the time code in hours, minutes and seconds, are placed in the first 20 (0 through 19) of the 25 index periods making up the frame. The REFERENCE MARK is placed in the last index period with the trailing edge "on time". Each index period contains ten carrier cycles. The bits representing by large cycles, as described above, are grouped at the ends of their respective index periods with the gaps between the groups of large cycles filled with smaller cycles.

The Reader Logic counts the $\overline{LLC}$ pulses. It interprets 8 or 9 pulses as a MARK, 5, 6 or 7 pulses as a ONE and 1, 2, 3 or 4 pulses as a ZERO, thus achieving a measure of digital filtering. When a MARK is detected, the shift-register is cleared, the Accumulator (see Chapter 5) is updated and a ONE is loaded into the shift-register. As each bit in the code is identified it is loaded into the shift-register behind this ONE, thus shifting it to the right. When the 20th bit (the last bit in the frame) is loaded in, the ONE appears in the 21st output position, opening a gate, resulting in the transfer of the contents of the shift-register into the Accumulator in bytes. This synchronizes the Accumulator with the incoming time code. Once synchronism has been achieved, this transfer does not change the contents of the Accumulator since it is updated at the beginning of the frame.

2) FUNCTION

Flip-flop U1-6,3 is set by the negative-going transitions of the EC signal. If a large cycle is present ($\overline{LLC}$ pulse) it immediately resets this flip-flop ($\overline{LLC}$ pulses are narrower and fall between the leading and trailing edges of the EC pulses). The resulting signal (H) maintains flip-flop U2-6, U3-6 in a set condition while $\overline{LLC}$ pulses are preset.

After H goes positive at the end of a $\overline{LLC}$ pulse group it permits the next positive transition of the EC signal to reset U2-6, U3-6. The output signal (I) sets flip-flop U1-8, 11 removing the clamp (signal J) from U3-6 permitting it to go to ground (signal K) when signal I returns positive. Signal K clamps U2-6, U3-6 in a set condition preventing any more I pulses from being generated until after another group of $\overline{LLC}$ pulses are received. Signal I is inverted by U17-4 and

fed to the shift-register as the shift-(clock) input. Signal K is used to reset the ONES flip-flop U3-11,8.

Decade U19 counts $\overline{LLC}$ pulses. At a count of five both inputs to gate U18-11 go positive and the output goes to ground setting the ONES flip-flop U3-11,8. The output (signal M) is fed to the input, to the first section of the shift-register, U7. When a MARK is received the ONES flip-flop is set at a count of five as described above. At a count of eight, output U19-11 goes positive opening gate U13-3. The inverse of the differentiated leading edge of this signal (signal S from U17-12) clears the shift-register. Gate U13-3 passes the next positive transition of the EC signal and the output (signal N) sets flip-flop U14-9 when it returns positive. Output U14-9 opens gate U13-11 to the next positive transition of the EC signal, the leading edge of which is on time. The resulting output is the 1 pps update signal which is fed to the Accumulator through buffer U16-3. It is inverted by U17-2 and ac-coupled to the $\overline{clear}$ input of flip-flop U14-9, resetting it on the trailing edge. This Reset pulse is also fed through gate U18-3 to the reset input of decade U19, thus removing the gate signal from U13-3. The ONES flip-flop remains set until after the shift pulse from U17-4 has loaded the ONE into the shift-register. It is reset by signal K as mentioned previously.

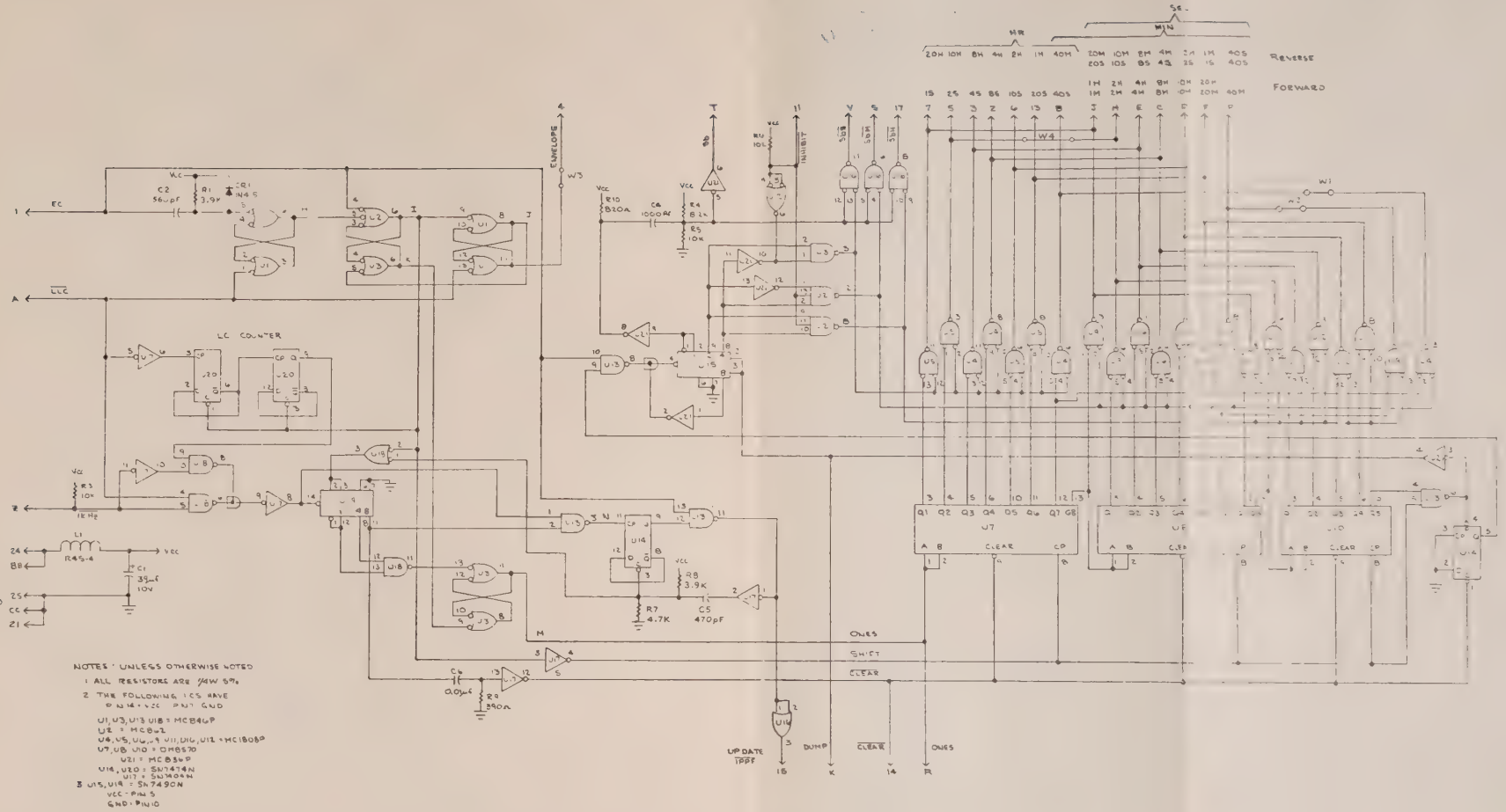
The 20 time code bits identified as ONES or ZEROS are loaded into the shift-register behind the ONE bit derived from the MARK. Here, a ONE consisting of 5, 6, or 7 $\overline{LLC}$ pulses sets the ones flip-flop as did the MARK. A ZERO is assumed to exist in the absence of a ONE, with the exception that at least one $\overline{LLC}$ pulse must be present or no shift pulse will be generated.

The shift-register consists of U7, U8 and U10 connected in tandum. When all 20 time code bits have been loaded, the ONE bit from the MARK appears at output U10-10 opening gate U13-6 to the coincidence shift pulse from U17-4. The output from U13-6 goes to ground setting flip-flop U14-5 and resetting counter U15 through U21-4.

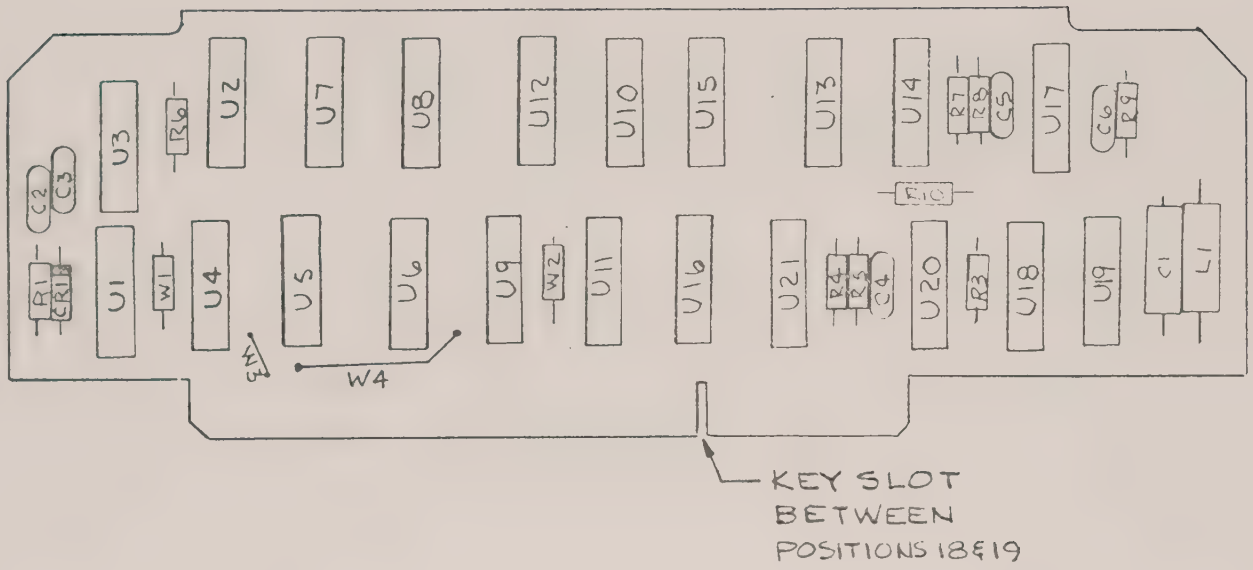
Counter U15 controls the scan gates U4, U5, U6, U9, U11 and U12) on the parallel output lines from the shift-register. It strobes the signals on these lines into the Accumulator in three bytes of hours, minutes and seconds.

The output from U14-5 opens gate U13-8 feeding inverted ED signals to U15. (Counter U15 was locked at a count of eight prior to being reset. This was accomplished by U21-2 which inverts the "8" bit, clamping the input at ground.) The "1" bit from U15 is inverted by U21-8 and differentiated, thus forming a strobe signal which is fed to three Strobe gates on U16. Only one of these gates is open at a time.

At a count of two the output from U3-3 goes to ground, opening the "seconds" scan gates on U4 and U5. At a count of five, the Strobe Seconds (SbS) signal is generated at U16-11. This signal loads the seconds data into the Accumulator. In like manner, the minutes data are prsented to the Accumulator at a count of four (Scan Gates on U6 and U9 open), and strobed (SbM output from U16-6) at a count of five. Hours data are gated at a count of six and strobed at a count of seven (Gates on U11 and U12, Strobe SbH from U16-8). At a count of eight counter U15 again locks as described previously. This completes one cycle of forward operation.



XR-3 READER LOGIC
#021658-7-1 REV F



ASSEMBLY XR-3 READER LOGIC #021658-4-1 REV D

PARTS LIST

READER LOGIC #021658-7-1 REV E

REF.	DESCRIPTION	SD PART NO.
	Assembly	021658-4-1
	Schematic	021658-7-1
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, 300 V, DM	100222
C4	Capacitor, 1000 pF, 100 V	100243
C5	Capacitor, 470 pF, 500 V	100221
C6	Capacitor, 0.01 µF, 100 V	100103
CR1	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1,8	Resistor, 3.9 k 5%, ¼ W	101601
R7	Resistor, 4.7 k 5%, ¼ W	101598
R3,5,6	Resistor, 10 k 5%, ¼ W	101570
R4	Resistor, 8.2 k 5%, ¼ W	101595
R9	Resistor, 390 Ω 5%, ¼ W	101592
R10	Resistor, 820 Ω 5%, ¼ W	101567
U1,3,13,18	Integrated Circuit, MC846P	019716
U2	Integrated Circuit, MC862P	019719
U4-6,9,11,12,16	Integrated Circuit, MC1808P	025734
U7,8,10	Integrated Circuit, DM8570	025751
U14,20	Integrated Circuit, SN7474N	025241
U15,19	Integrated Circuit, SN7490N	025732
U17	Integrated Circuit, SN7404N	025779
U21	Integrated Circuit, MC836P	025704
W1,2	Jumper, Molded	102879
W3,4	Jumper	
	Extractor	100865

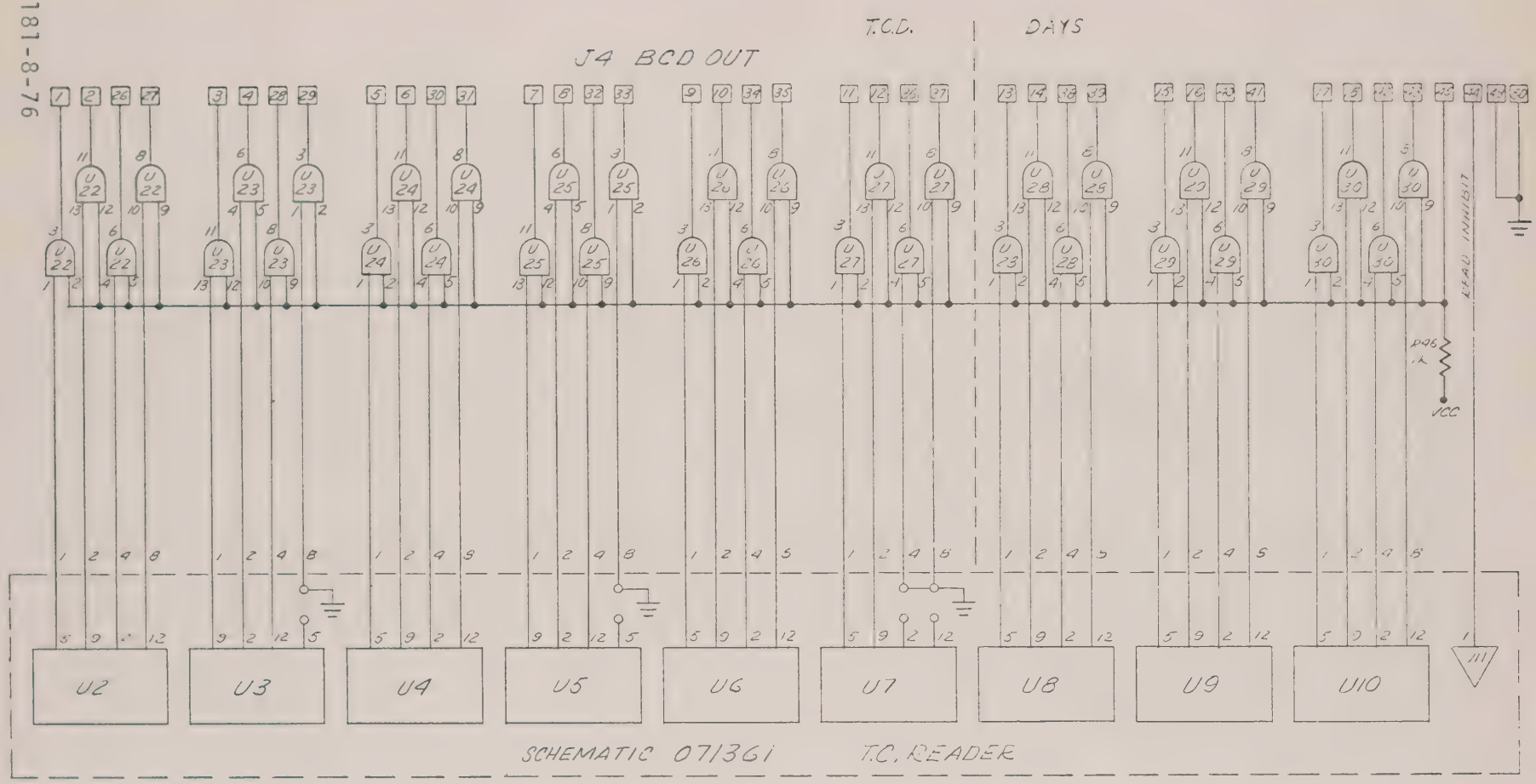
CIRCUIT DESCRIPTION
PARALLEL BCD OUTPUTS (OPTIONS D11/D11D)
SCHEMATIC #7-071449

1) GENERAL

Options D11 and D11D provide buffered parallel BCD outputs through rear panel connector J4.

2) CIRCUIT DESCRIPTION

Option D11 adds buffer chips U23 through U27 to the basic unit to provide BCD time-of-day (TOD) in hours, minutes and seconds. Dummy bits are included. Option D11D adds buffer chips U28 through U30 for three digits of days. Days Option E13 must be included as a prerequisite. A Read Inhibit input is provided at J4-44 which may be used to freeze the time in the Accumulator when pulled high. A gate input at J4-45 forces all parallel BCD output lines low when pulled to ground.



NOTE:
1. RESISTORS ——— ¼W, 5%.
2. U22 THRU U30 —— MC 1806 P.
   PIN 7 GND
   PIN 14 VCC

SCHEMATIC PARALLEL BCD OUTPUTS #7-071449 REV A

PARTS LIST

BCD OUTPUT

REF.	DESCRIPTION	SD PART NO.
	OPTION D11/D11D	
	ADD	
	Schematic	7-071449
J4	Connector, 50 pin, 57-40500	101156
P4	Connector, 50 pin, 57-30500	101157
	Connector, Mounting Plate	071354
R46	Resistor, 1 k 5%, ¼ W	101569
U22-27	Integrated Circuit, MC1806P	025733
	DELETE	
	Connector, Cover Plate	071355
	* * * * * * * * * *	
	OPTION D11D	
	ADD	
U28-30	Integrated Circuit, MC1806P	025733

CIRCUIT DESCRIPTION
DAYS (OPTION E13)
SCHEMATIC #7-071361

1) GENERAL

Option E13 extends the Accumulator and Display to include three additional digits.

2) CIRCUIT DESCRIPTION

See Chapter 5.

PARTS LIST

DAYS OPTION #071475 REV B

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-071361
U8-10	Integrated Circuit, N8280A	025722
U19-21	Integrated Circuit, DD700	045203
V7-9	Beckman Display, SP-101	116082

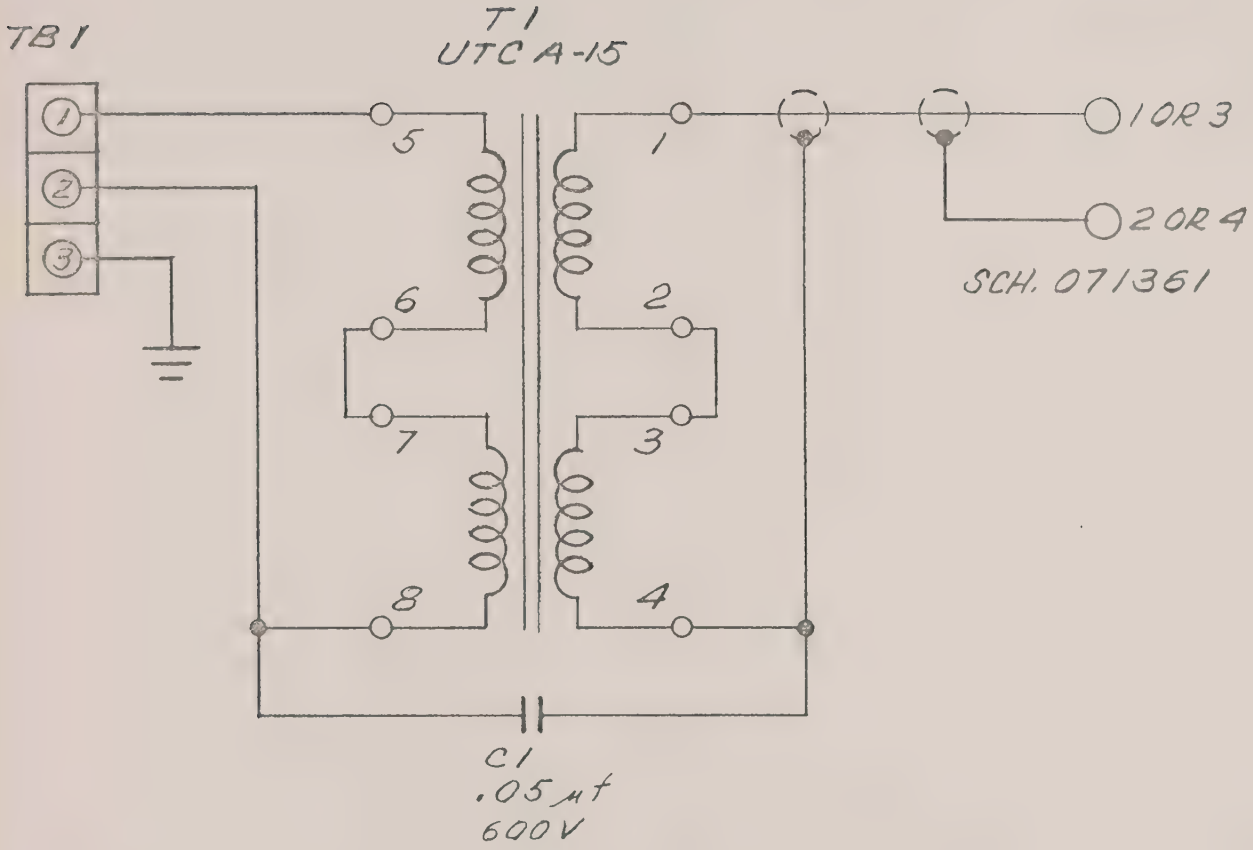
CIRCUIT DESCRIPTION
TRANSFORMER INPUT OPTION
SCHEMATIC #7-071454

1) GENERAL

This option adds rear panel terminal strip TB1 and input transformer T1 to the basic unit. Input BNC's J2 and J3 are deleted.

2) SPECIFICATIONS

With the input transformer installed, the modulated input code can be accepted with a carrier frequency from 80 Hz to 12 kHz and a modulation ratio between 2:1 and 6:1. Input levels of -20 dbm to +10 dbm (0.25 to 7.5 volts peak-to-peak) can be decoded. The input is floating and has a bridging impedance at 1 kHz of greater than 10 k ohms. DC input resistance is infinite.



SCHEMATIC TRANSFORMER INPUT #7-071454 REV A

PARTS LIST

TRANSFORMER INPUT OPTION #071473 REV A

REF.	DESCRIPTION	SD PART NO.
	Schematic	7-071454
C1	Capacitor, .05 µF, 600 V, Disc	100074
T1	Transformer, UTCA15	102892
T1	Transformer Bracket	03126511
TB1	Barrier Strip	100483
	Cinch, JO3-140Y	

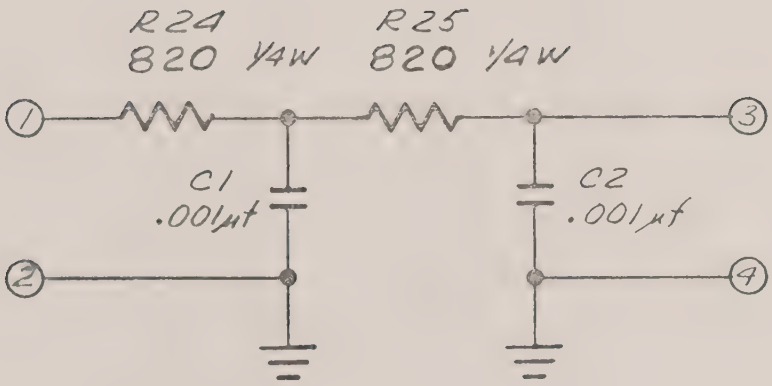
CIRCUIT DESCRIPTION
INPUT FILTER OPTION
SCHEMATIC #7-071472

1) GENERAL

This option adds a two pole low pass filter to the basic unit. It may also be combined with the Transformer Input Option.

2) SPECIFICATIONS

The filter is down 3 db at approximately 36 kHz with a rolloff of 20 db per decade.



SCHEMATIC FILTER OPTION #7-071472 REV A

PARTS LIST

FILTER OPTION #071471 REV A

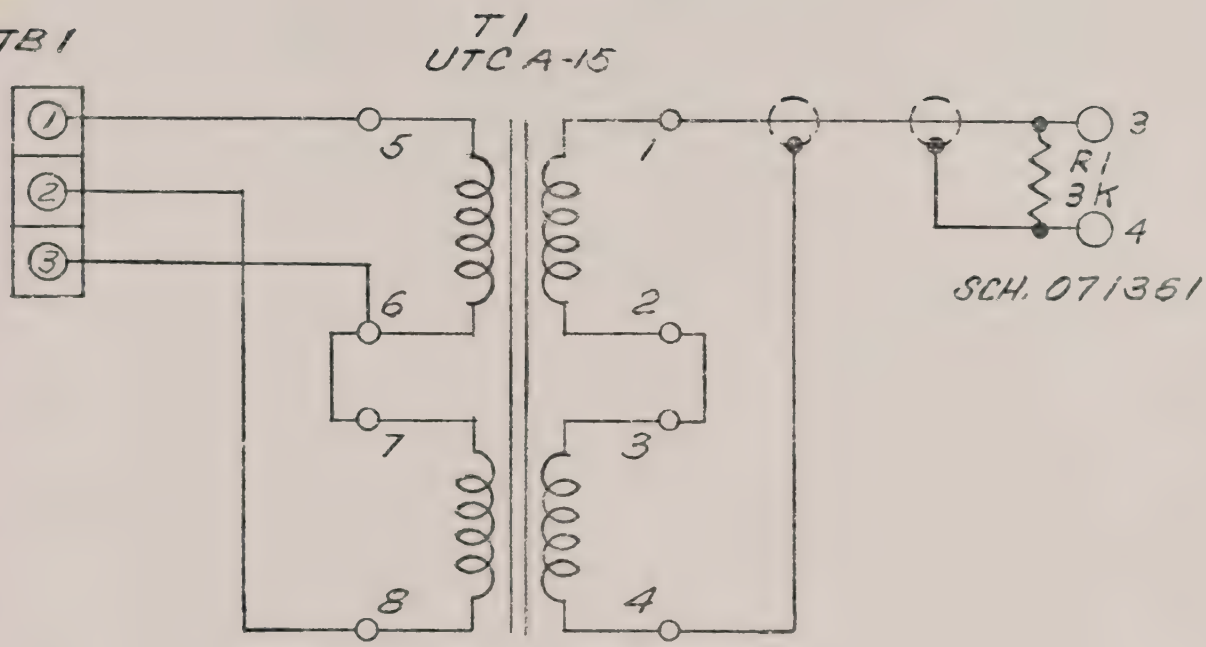
REF.	DESCRIPTION	SD PART NO.
	Schematic	7-071472
C1,2	Capacitor, Mylar, .001 µF, 100 V	
R24,25	Resistor, 820 Ω 5%, ¼ W	101567

CHAPTER 7
SPECIAL MODIFICATIONS

7.1 GENERAL

Modifications to the Model 8181, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

REV	DESCRIPTION	BY	CHK	DATE	APP'D
A	RELEASED TO RECORDS				



NOTE: J2 & J3 ARE REMOVED

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

...ced under United States Government Contract No. ... not be either released outside the Government or used, duplicated or disclosed in whole or in part for manufacture or procure... without the written permission of Systron-Donner Corporation ... for (1) emergency repair or overhaul work by or for the gov... ment where the item or process concerned is not otherwise ava... ly and able to enable timely performance of the work, or (2) ... be a foreign government and that the ends of the United States ... equire, provided that in either case the released, use, duplication ... disclosure hereof shall be subject to the foregoing limitations. This ... shall be marked on any reproduction hereof in whole or in part.

			SYSTRON DONNER CORPORATION CONCORD CALIFORNIA	TRANSFORMER INPUT OPTION SCHEMATIC ECO RELEASED
			CODE IDENT 53947	
8151				
APPLICATION			MATERIAL	DEPT. 071 SIZE A PART NO. 07-473-2A

PARTS LIST

TRANSFORMER INPUT OPTION #07147302 REV A

REF.	DESCRIPTION	SD PART NO.
	Schematic	7-07147302
R1	Resistor, 3 k, 5%, ¼ W	101913
T1	Transformer	102892
TB1	Strip, Barrier	100483
	Bracket, Transformer	03126511
	Plug, Hole	100952
	DELETE	
J2,3	BNC	101155